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QUESTION N° : Q3

Metal Vapor Deposition & High Electrical Stress

Metal shielding protects alumina ceramics insulators of vacuum interrupters (VI) from metal vapor depositions (MVD). Generally, VI designs allow some MVD on the ceramic.

This MVD on ceramics degrades the insulation and reduce HV performance of the VI. The transition layer of highly conductive MVD to highly resistive ceramic can result in high electrical stress leading to dielectric breakdown.

Discrete regions arced during resistance measurement.

Therefore, a shield-less design will experience more voltage stress compared to a shielded one

Contribution to decarbonization, decentralization, and digitalization of Power Grid.

MVD pattern and its variation depends on internal geometry of the VI.

Short HV discharges are indicative of dielectric stress in the device.

Transition layers are under higher electrical stress more leading to dielectric breakdown.

Controlling MVD pattern can help developing cost-effective designs for lower to higher ranges of VIs. Dielectrically improved VIs can potentially replace other modes of switching which can adversely affect the environment.

Voltage collapse phenomenon may generate a pattern. The pattern of discharge, its frequency, intensities may indicate distress. More studies can be carried out to capture such data with controlled variations and establish alarms or alerts for remote and predictive maintenance of the system.