Paris Session 2022

cigre
For power system expertise

EXPECTED DIFFICULTIES OF LINE CURRENT DIFFERENTIAL RELAYS WITH PROCESS BUS APPLICATION ~WHOLE SYSTEM SYNCHRONISATION~

SC B5 PS2 Q2.01

What are the challenges in the development of digital substations and how to address the problems caused by the digitalization?

Ryosuke KUNIYOSHI (JAPAN)

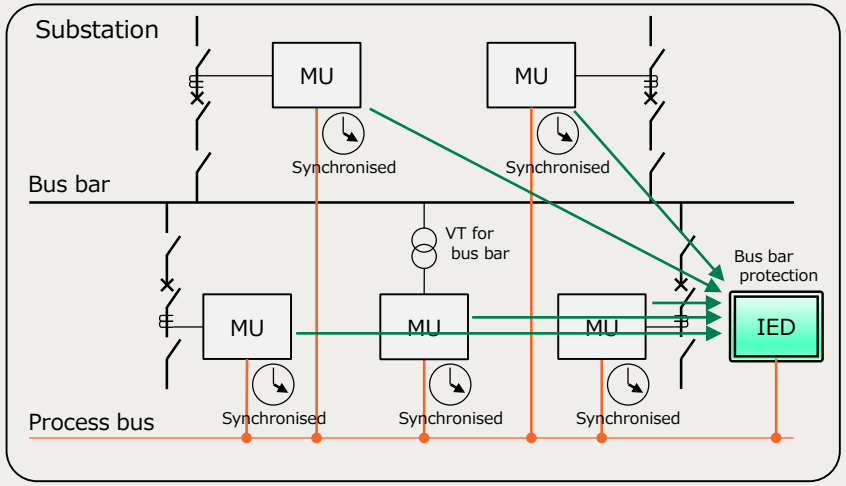
Kansai Transmission and Distribution
Kansai Electric Power Group power with heart

Sampling synchronisation in process bus system with conventional line current differential relays

(A) Station-wide synchronisation caused by Process Bus

With process bus system, sampling synchronisation throughout the substation is necessary

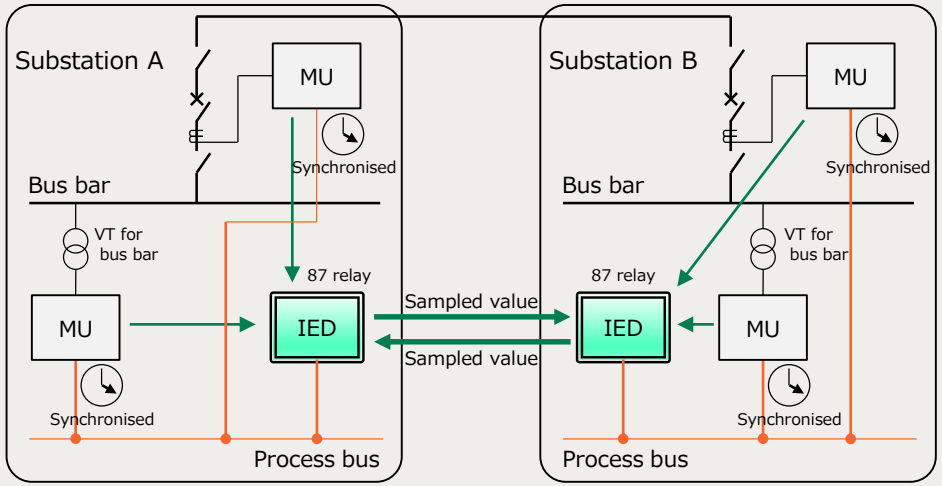
- Sampled element: Voltage (**V**) & Current (**I**)
- Calculated operation value:
  Impedance (**Z**), Differential current (**ΔI**),
  Active power (**P**) / Reactive power (**Q**), …



(B) Pair-substation synchronisation caused by 87 relay

With line current differential relays, sampling synchronisation between both substations is necessary

- Sampled element: Current in A S/S ($\mathbf{I_A}$), in B S/S ($\mathbf{I_B}$)
- Calculated operation value: Differential current (**ΔI**)



• Whole-system synchronisation

MUs in whole system is to be synchronised

Involves difficulties

Group Discussion Meeting

87 relay: Line current differential relay
S/S: Sub station MU: Merging Unit

DIFFICULTIES: Have to consider "whole-system synchronisation" for combination of process bus and line current diff. relays

To archive "whole-system synchronisation",
time synchronisation protocol is used in general

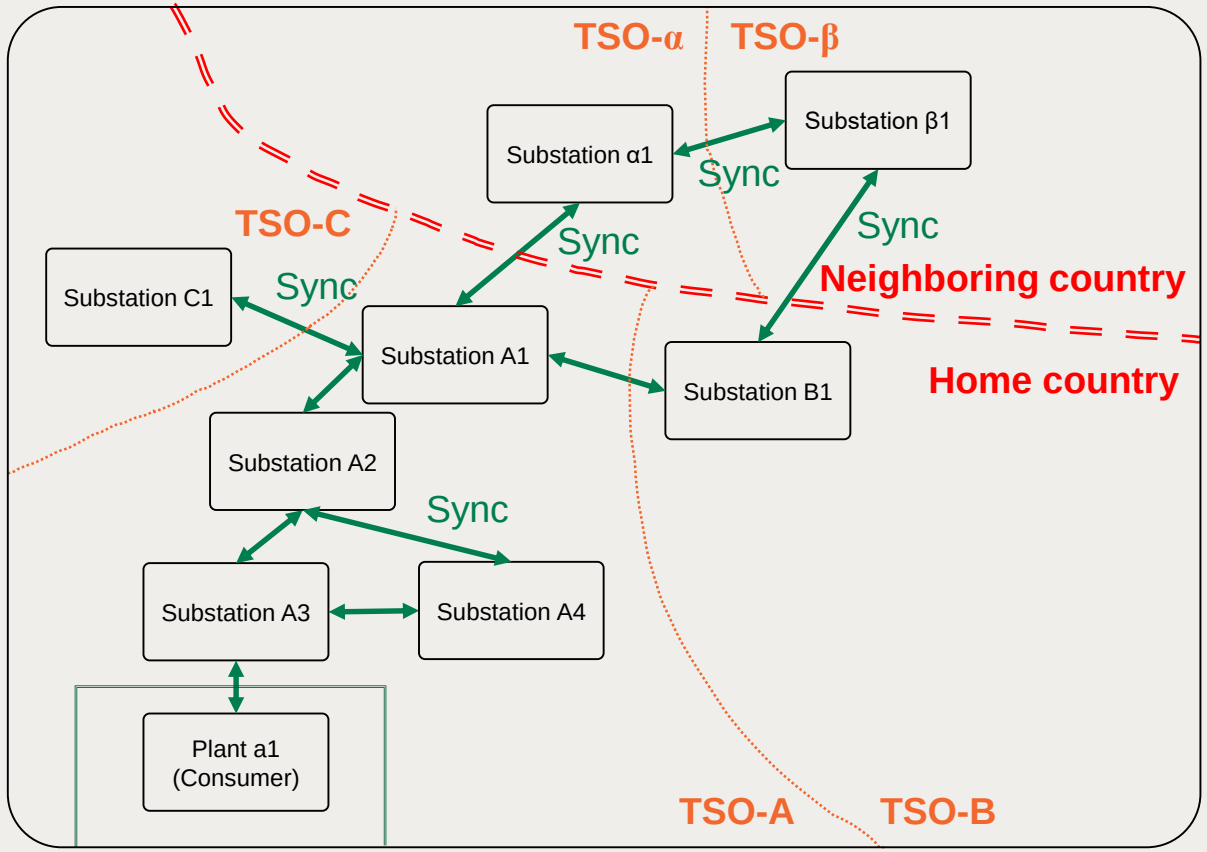
- What is the problem of "Whole-system synchronisation"?

(for technical reason)

- Who (which company) control GMC?
  When the grid is widely interconnected
- Where GMC be placed?
  Need to consider natural disaster
- How GMC determine time?
  GPS / Radio clock / Atomic clock / Quartz clock …
- Which neighbour clock should it trust

(for security reason)

- Interconnected to other company / country
- System cannot be standalone



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GMC: Grand master clock
87 relay: Line current differential relay

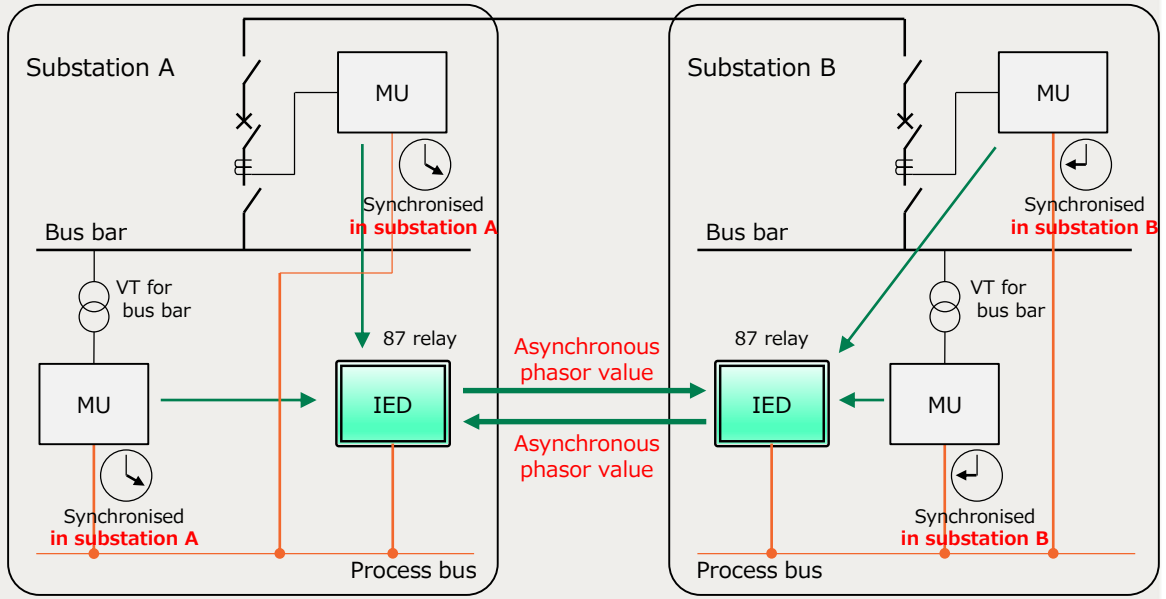
SOLUTION: Avoid “whole-system synchronisation” by “Asynchronous line current differential relays”

- Asynchronous line current differential relays
  - Sampling timing can be different in each terminal
  - Transmit phasor value with relevant to characteristic vector to other terminals
  - Conditions of communication lines such as jitter or latency difference in up / downstream are unnecessary

- “Station-wide synchronisation” with asynchronous relays
  - ✔ The MUs in Substation A are synchronised
  - ✔ The MUs in Substation B are synchronised
  - ✔ The MU in Substation A and in Substation B are **NOT** need to be synchronised

The segment of sampling synchronisation is limited to each substation

“Whole-system synchronisation” is avoidable



Group Discussion Meeting

87 relay: Line current differential relay