

Compensation Method to speedup offline and real-time Electromagnetic Transients simulation of inverter-based transmission networks

Needs of offline and real-time Electromagnetic Transients simulation at RTE

In the scope of Energy Transition, more power electronics equipment are installed in the French Network to integrate renewable resources and to strengthen interconnection power capacity between European countries. This raises new challenges for RTE, the French Transmission System Operator (TSO) in terms of network stability [1]. Potential interactions between power electronics equipment have to be studied which involve ElectroMagnetic Transients (EMT) phenomena. There is a need of using EMT simulation tool to handle those risks. Offline EMT simulation with detailed modelling able to have a good accuracy. Real-time simulation through HIL (Hardware-In-the-Loop) interacts with control replicas which are an exact copy of protections and physical controllers installed on-site. Having the real control in the simulation loop improves the accuracy being closer to on-site phenomena. RTE has built a real-time simulation lab nearby Lyon, Campus Transfo, to host control replicas of each power electronics projects such as Static Var Compensators (SVC) or High Voltage Direct Current (HVDC) interconnections. In order to have a good accuracy by using detailed modelling, lower time-steps, used to integrate numerically network equations, are required. This slows down the simulation and in real-time the same modelling cannot be kept without respecting the time constraint. Solutions have to be found to reduce the simulation computation time.

Parallelization Techniques to speedup EMT simulations

Parallelization techniques are key methods to accelerate EMT simulations. Traditional techniques are delay-based. They are widely used in EMT simulation tools. Propagation delays of power lines, Line-Delay (LD) method, allow to decouple network solution. If this propagation delay is higher than the simulation time-step, the same accuracy is kept as there is enough delay to exchange valid computed data for the next time-step. However, for power electronics-based networks, physical delays are not always available for parallel decoupling. For those cases, stubline (SL) or TLine [2] can be used instead. It consists to introduce an artificial power line delay for having an equivalent decoupling to LD method. With this SL method, the accuracy is not guaranteed as the network solution is no longer simultaneous. Delay-free techniques have to be considered. Recently, the Compensation Method (CM), one of these techniques, has been implemented and tested in [3] to speedup inverter-based transmission networks. It is based on Thevenin equivalent principle and superposition theorem. It can split everywhere a network solution and reconcile the dynamic of both decoupled subnetworks.

Parallel offline and real-time simulations of Eleclink HVDC interconnection using Compensation Method

Eleclink [4] is a Voltage Source Converter (VSC) - HVDC interconnection between France (Peuplingues) and United Kingdom (Cheriton) in operation since 2022. It is composed of a 1000 MW symmetrical monopole based on Modular Multilevel Converter (MMC) technology from Siemens. The DC operating voltage is set to ± 320 kV. The same converter model of [5] is used for offline and real-time simulations (HYPERSIM). A generic HVDC control is imported from Matlab/Simulink. Frequency dependent cable models are used to represent the long DC cables. The 400 kV AC grids are modeled with Thevenin short circuit level equivalents. The time-step is 10 μ s. A 20 s simulation runs the starting sequence on an OP5142 target 32 bits Linux with 24 cores (2 CPU Intel Xeon X5690 3.5 GHz - 12 cores). The power flow from France to UK is set to 500 MW. First, LD method is used to decouple the network through DC cables. Then, further decoupling can be done with CM (LD+CM) or SL (LD+SL) to split converter modelling from AC network as depicted in Figure 1. Inductance values for stublines are set to 1 mH with a small resistance ($1e-6 \Omega$). Five cores are required for LD case and seven cores for LD+CM and LD+SL. Table 1 shows the performance during offline simulation. It indicates also if the 10 μ s time-step is respected during real-time simulation. LD is not enough to run this modelling in real-time. LD+CM and LD+SL speedup the offline simulation. Then, real-time simulation can be performed without any overruns. As SL introduces artificial delay, the accuracy of the simulation decreases. In steady state (Figure 2), higher oscillations can be observed in the DC voltage whereas a perfect match is obtained for CM. LD+CM can be selected to have a faster and an accurate simulation of this modelling in both offline and real-time simulations.

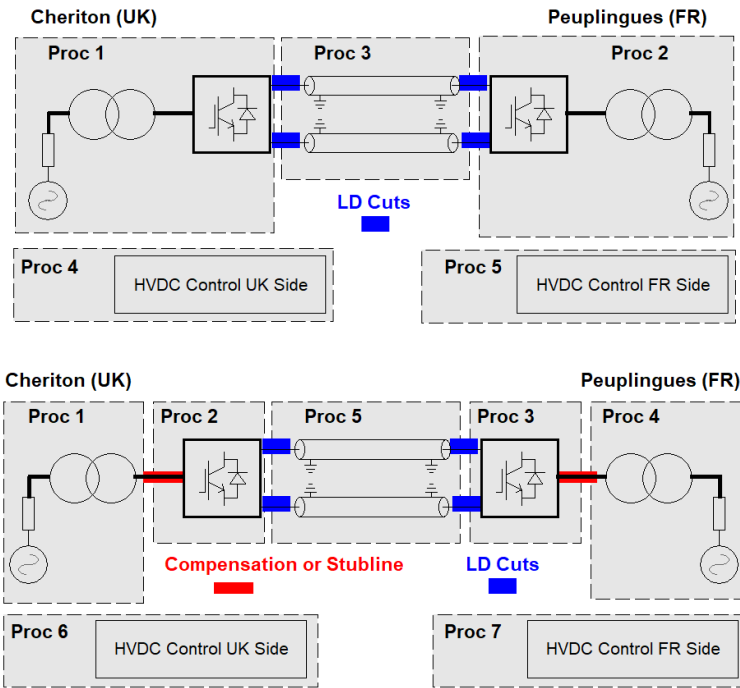


Figure 1: Overview of Eleclink modelling and parallel decoupling for LD (top), LD+CM and LD+SL (bottom).

Parallel Solutions	Offline		Real-time 10 μ s
	Computation time (s)	Speedup	
LD	16.2	1.0	No
LD+SL	10.6	1.5	Yes
LD+CM	11.6	1.4	Yes

Table 1: Performance of each parallel solutions for the 20 s starting sequence.

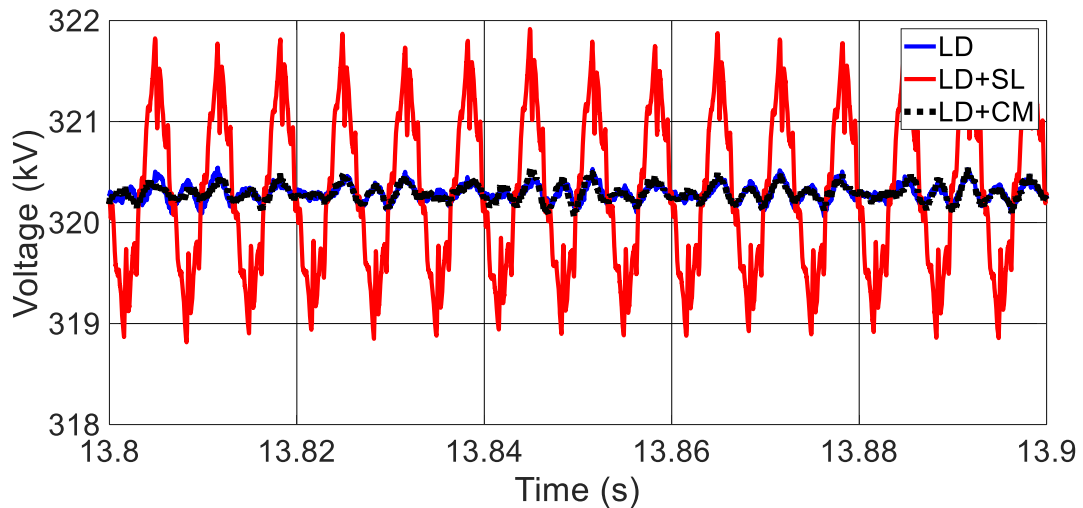


Figure 2 : DC Voltage for LD, LD+SL and LD+CM.

References

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