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Recent HVDC Circuit Breaker Development and Testing

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SUMMARY

The paper provides an overview of the complete research and development track that led to the public demonstration of three different technologies of HVDC circuit breakers (CBs), which are in the last stage of their product development. Accordingly, the fault current interruption of the following CB technologies from three different vendors has been demonstrated:

- Active current injection technology
  - Direct discharge of pre-charged capacitor-based injection technology (160/200 kV, 16/20 kA)
  - Voltage source converter (VSC) assisted resonant current injection technology (80 kV, 12/15 kA)
- Hybrid technology (350 kV, 20 kA)

The lessons learned are useful input to the ongoing international standardization activities dealing with the development of test requirements for HVDC CBs. HVDC grids are in operation in China and are on the horizon in Europe due to plans for large-scale renewable energy resource integration to enable carbon neutrality by 2050. Since operational experience with the protection of HVDC grids is almost non-existent, simulation models of conceptual HVDC grids are used to study the impact of faults on such grids. Such simulation studies are used to quantify the electrical transient stresses to which an HVDC CB is subjected. As a result, quantities like maximum fault current as well as the rate-of-rise, the magnitude and duration of the transient interruption voltage (TIV), and the energy to be dissipated are evaluated and used to define the test requirements. Moreover, an experimental HVDC CB is set up in a high-power laboratory to investigate the impact of HVDC fault current interruption on the key CB components. The results of this investigation are used to justify the test requirements. Next, based on the test requirements, a detailed test procedure is set up, consisting of clearly defined test-duties, to be followed in order to qualify the breaker for its main task: the fault current interruption under full power condition. These test requirements and procedure were agreed among the manufacturers of the three technologies of HVDC CBs in the project. In addition, a study evaluating the practical aspects as well as comparing the performance of several possible test circuits was carried out. A test circuit based on low-frequency AC short-circuit generators was identified as the most pragmatic option to replicate the short-circuit interruption stresses as in service. Finally, all the three technologies, with rated voltages up to 350 kV and fault current interruption ratings up to 20 kA were demonstrated regarding their fault interruption capability, using the defined test-requirements. The demonstrations were performed in the presence of different stakeholders such as transmission system operators, project developers and other possible users of HVDC CBs. For all CB technology demonstrations, it was the first time a complete breaker prototype was submitted to a complete set of full-power test stresses in a single shot interruption test. This paper shares test results and experience gathered.

KEYWORDS

HVDC Circuit Breaker, Multi-Terminal, HVDC Grid, Short circuit, Testing

I. Introduction

HVDC grids are in operation in China and are on the horizon in Europe due to plans for large-scale renewable energy resource integration [1], [2]. HVDC grids require a high-speed protection system (consisting of relays and fault clearing devices such as HVDC circuit breakers (CBs)) that detects, locates, and isolates a fault within several milliseconds. HVDC CBs have been subject to significant research and development over the last few years [2]- [3]. Recently, a few products have been deployed in multi-terminal HVDC pilot projects in China. To date, 20 HVDC CBs based on different current interruption techniques with ratings in the range of 160 – 500 kV have been installed.

Unlike an HVAC CB, an HVDC CB is not just a simple mechanical contact system, but rather a system of components arranged in three parallel current branches (continuous current branch, commutation branch(es) and energy absorption branch), to which current is commutated in a predefined sequence to achieve DC current interruption. Moreover, for (extra-)high-voltage applications, HVDC CBs are designed in a modular approach, where several components are combined in series either per current branch(es) or as independent HVDC CB modules [4].

Two leading technologies; namely, the mechanical active current injection HVDC CB and the hybrid HVDC CB have become the preferred candidates for HVDC grids. The gap in performance between these technologies is narrowing, and in some cases similar performance requirements have been set and met [3]. Nevertheless, each technology has its own pros and cons which can be further developed [2].

In all HVDC CBs, a fast mechanical switchgear is present either to interrupt and/or isolate. This component determines the speed of operation, which is a crucial parameter, of the breaker. To achieve fast contact separation, electromagnetic pulse drive mechanisms are used instead of conventional spring, hydraulic or magnetic drives. To cope with high-voltage withstand in open position, several series connected switches may be necessary [5], [3]. In this case synchronous operation (opening), equal voltage distribution and power supply at different potentials are the main challenges [2], [4]. In general, optimization studies are needed towards reduction of cost, number of parts, which in some designs can be significant [2].

This paper summarizes the work performed within the framework of the recently (2020) concluded EU funded PROMOTioN project [6] that led to the performance demonstration of HVDC CBs developed by three original equipment manufacturers (OEMs). The demonstrations were performed in the presence of different stakeholders such as transmission system operators, project developers and other possible HVDC CBs users witnessing the live test at the KEMA high-power laboratory in Arnhem, Netherlands. In all cases, this was the first time a complete HVDC CB prototype was submitted to a full-power test.

The remainder of the paper is organized as follows. Section II summarizes the fault current simulation studies performed on a hypothetical HVDC grid. A summary of fault current interruption by models of HVDC CBs is discussed in Section III. The critical stages of fault current interruption and the key stresses at each stage are briefly presented together with the agreed upon test duties of HVDC CBs. In Section IV the test method and the designed test circuit is briefly elaborated. This is followed by the discussion of the test results of the three publicly demonstrated HVDC CB technologies in Section V. Finally, conclusions based on project results discussed in the paper are presented in Section VI.

II. Summary of Fault Current Simulation Studies

In the absence of operational experience, the effective approach to define the requirements of HVDC CBs is to perform system simulation studies. In this project, one of the tasks was aimed at identifying the factors that determine the fault currents in meshed HVDC grids. Fault analysis has been carried out by simulation of a hypothetical five-terminal, ±320 kV HVDC benchmark network (with bipolar converter configuration) shown in Figure 1. It is based on the state-of-the-art half-bridge (HB) modular multi-level converters (MMC) represented by the detailed equivalent model [7].

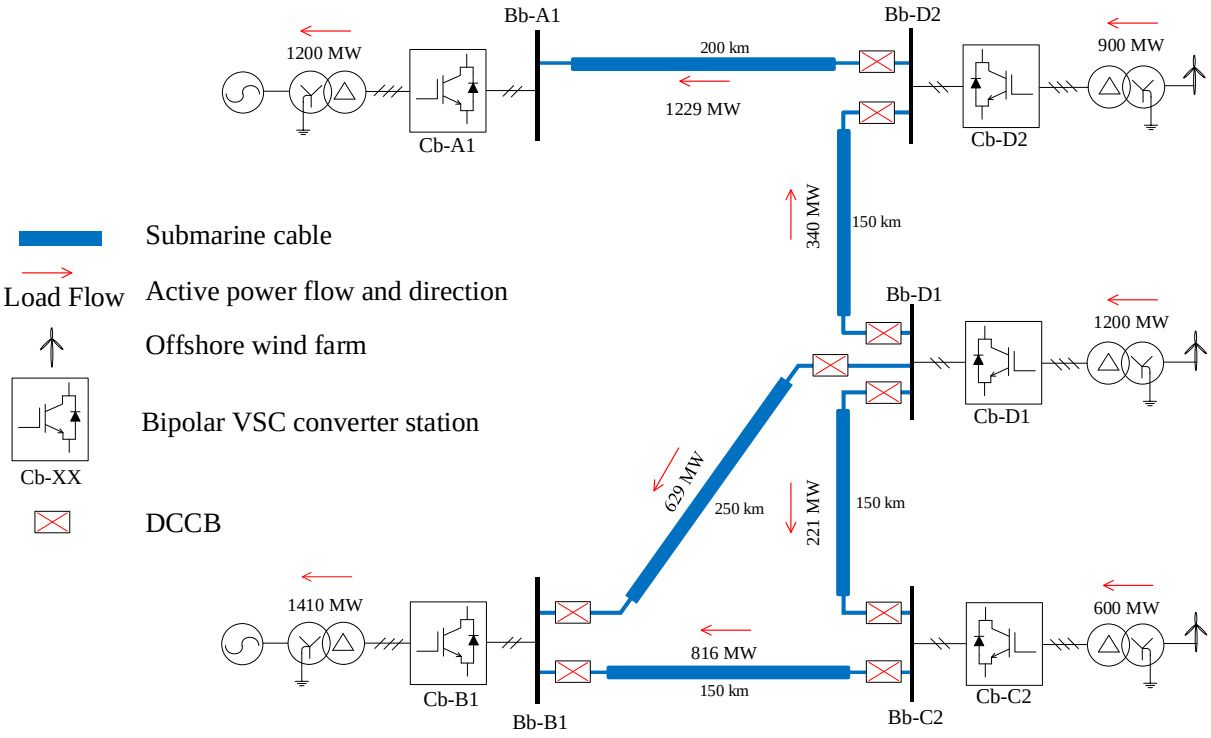

Figure 1: Five terminal 320 kV bipolar HVDC benchmark grid for fault simulation studies

A pole-to-ground fault is applied on a positive pole cable between converters Cb-D1 and Cb-B1. The major events during fault current build-up are identified in three distinct stages: namely, sub-module (SM) capacitor discharge, arm current decay and AC in-feed [8]. During the SM capacitor discharge stage, the fault current is mainly supplied by the converter directly connected to the DC bus at the end of the faulted line. During the arm current decay stage, the discharge from other feeders connected to the DC bus becomes prominent. The strength of the AC grid and the impedance of the converter transformer become dominant factors during the AC in-feed stage. The overall current through a CB on a faulted cable increases with the number of cables connected to the DC bus. It also concluded that considering the breaker operation times of the recently developed HVDC CBs, a fault close to a converter terminal with multiple connections results in the worst-case fault current.

III. Summary of Fault Current Interruption by HVDC Circuit Breaker

The models HVDC CBs developed using realistic parameters are embedded into the benchmark HVDC grid model to investigate the interactions of the HVDC CBs with the system as well as to quantify the electrical stresses during fault current interruption. HVDC CBs are placed at each end of the HVDC cables together with current limiting reactors to implement a fully selective fault clearing strategy.

Figure 2 shows the current interruption process by an active current injection HVDC CB along with the associated stresses during the current interruption. Under normal operation, the capacitor of the CB is pre-charged to the system voltage (−320 kV). It is assumed that local current interruption in the continuous current branch is achieved upon the first zero crossing of the injected current. A fault neutralization time of 9 ms, of which 2 ms is the relay time, is assumed in the simulation. In order to limit the fault current to less than 16 kA over this period, a 150 mH current limiting reactor is placed in series with the HVDC CB.

In all HVDC CBs the fault current breaking strategy involves local current interruption in the continuous current branch followed by internal current commutation to the branch(es), which generate the TIV and ultimately current commutation into the energy absorption branch. One of the main differences between AC and DC current interruption is that in the latter case the system voltage starts to recover not at the

end of the current interruption process but rather from the moment the HVDC CB starts to generate the counter voltage (TIV). That is while the fault current is still at its peak – see the top graph of Figure 2. As a result of this, there is significant electrical energy contribution from the system during the current suppression period. Thus, it is not only the system's magnetic energy stored in the current limiting reactor that the CB must absorb but also the electrical energy supplied by the system during the fault current suppression period– see the energy decomposition in the bottom graph of Figure 2. Due to the system voltage recovery during the energy dissipation phase, the energy coming from the grid in most cases is larger than the energy stored in the current limiting reactor [4], [8].

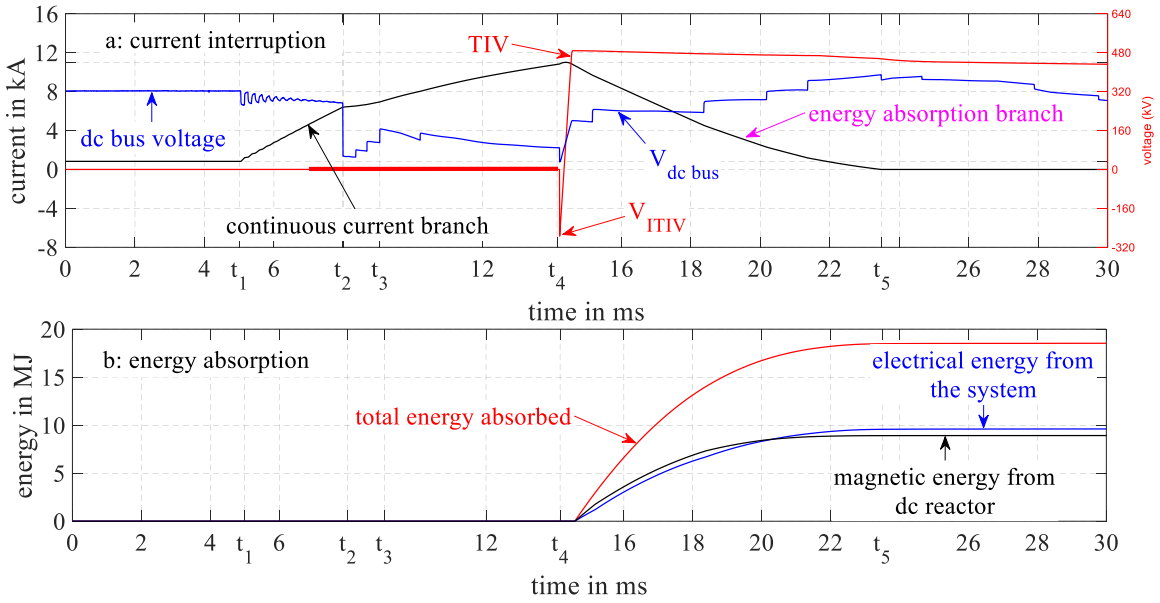

Figure 2: Stresses on active current injection HVDC CB. a: Current through and voltage across the CB during interruption, b: Energy absorbed by CB *[8]*

IV. Stresses and Critical Stages of DC Short-Circuit Current Interruption

In HVDC CBs, a whole class of new technologies are combined and coupled mechanically, electrically and thermally. Several commercially available (sub)components for standard applications are being applied in a non-standard manner. Two sets of stresses to the HVDC CB components have been identified: electrical stresses and non-electrical stresses. Referring to Figure 2, the basic electrical stresses on an HVDC CB that need to be reproduced during a short-circuit current interruption test are:

1) **Current stress** – the maximum breaking value with proper rate-of-rise. Moreover, the trajectory of current is essential, for example, for the thermal stresses of arcing mechanical gaps or of the power electrotonic (PE) switches. The rate-of-rise shall be determined based on the worst-case relay time and internal current commutation time so that the test current covers all the possible short-circuit currents in the system. Moreover, the capability to interrupt low-current and continuous current shall be verified.
2) **Voltage stress** – this includes the TIV (also the initial TIV in some cases) during the dynamic/opening process and the DC recovery voltage that appears after an HVDC CB has isolated the faulty section from the rest of the system.

Non-electrical stresses are:

1) **Thermal energy stress** – the dissipation of energy during the current suppression period leads to thermal stress of the energy absorption branch of the HVDC CB while the mechanical and/or the PE components in the other branches are at the same time electrically stressed by the sustained TIV. The capability to absorb the thermal energy, released during the fault current suppression period is of key importance during a short-circuit current interruption test and requires high testing power.

2) **Mechanical stresses** – this is to verify the mechanical consistency, integrity, stability of the mechanical switching gaps that are common to all HVDC CBs for reducing losses. All mechanical switching devices are built upon high-speed actuators that are new to the industry. There are several breaker designs that needs to connect tens of mechanical switches in series for interruption/insulation to achieve the higher rated voltage such as 320 kV and 525 kV.

To stress the HVDC CBs as in service during a test, a test circuit should provide sufficient current, voltage and energy. The specific details are mainly dependent on the system under consideration. The key functionality of any HVDC CB is to suppress the fault current to a negligible value in as short a duration as possible. The critical stages and the essential performance parameters that need to be demonstrated by an HVDC CB during a short-circuit current interruption test are:

1) **Internal current commutation** – capability to create a local current zero without restrike/breakdown of mechanical switches/interrupters or thermal overload of the PE components at the rated DC fault current interruption capability. The key design parameters (performance indicators) at this stage are:
    a. **Internal current commutation time** – the time from trip command until the peak value of interruption current is reached.
    b. **Maximum breaking current** – the maximum short-circuit current that the breaker can interrupt within the internal current commutation time. Moreover, the test current trajectory must encompass the system fault current excursions to ensure sufficient thermal stresses to the internal (sub-)components.
2) **Generation and maintenance of the TIV** – sufficient rate-of-rise and magnitude to initiate fault current suppression. Although determined by the CB itself, the rate-of-rise, the peak and the duration of the TIV are crucial parameters during a test.
3) **Energy absorption** – capability of energy absorption components to withstand thermal as well as dielectric voltage stress during fault current suppression. Depending on the rated sequence, this capability must be demonstrated several times within a defined sequence.
4) **DC recovery voltage withstand** – after current suppression, the breaker must withstand the rated maximum continuous DC voltage (up to 1.15 p.u.) for a certain duration until the residual current breaker opens (for example, 300 ms as in AC standards).

Although DC short-circuit current interruption has been the main focus of this contribution, there are other important tests including dielectric tests and operational tests, which are covered by the upcoming international standard IEC 62271-5. The number of breaking operations that the CB can perform before thermal degradation/damage occurs to its MOSA as well as the interruption intervals need to be defined. Moreover, the HVDC CBs are typically realized by connecting several modules in series to achieve high-voltage rating [6]. Interruption tests can be performed on a single module or multiple modules.

Table 1 presents a list of test-requirements agreed among the OEM partners of the project. The list contains three type of tests: fault current (TF100)-, continuous current (TC100)- and low-current (TC10) tests. These test duties correspond to the rated maximum fault current, the rated load/continuous current and 10% of the rated continuous current interruptions, respectively.

Table 1: Current breaking test duties. All tests are single opening operations

Test Name	Breaking current[1]	Remark	# of tests[2]
TC10±[3]	10% of rated continuous current	Low current interruption capability	4

[1] In all tests, DC recovery voltage ($U_{DC,}$ considering 10-15 % continuous operational overvoltage) will be supplied during at least 300 ms after main current interruption
[2] Half for forward current breaking and half for reverse current breaking
[3] ± indicates reverse and forward current breaking tests

TC100±	100% of rated continuous current	Rated current breaking current capability	4
TF100±	100% of peak fault current	Maximum current breaking capability at rated energy absorption	4

V. Test Circuit Based on AC Short-Circuit Generator

Ideally, HVDC CBs are tested using a high-power DC source, supplying high-current and high-voltage simultaneously, but are not economical and thus not available at any test laboratory worldwide. It was clear from the early days of HVDC CB development that it is unlikely that such an expensive and elaborate test circuit will be set up for solely testing HVDC CB prototypes [9], [10]. Thus, alternative test circuits providing equivalent stresses are sought. With this regard, different kinds of test circuits have been used at different stages of HVDC CB development [9], [11]. Various approaches (test methods) have been considered to address some of the limitations of the test circuits or to meet some of the essential stresses that need to be replicated in a test.

Within this project, candidate test circuits for HVDC CBs have been reviewed, evaluated, and compared on the basis of not only whether a given test circuit can supply the necessary stresses but also on the basis of availability, practical and economic feasibility. These test circuits include a high-power rectifier, a high-voltage charged capacitor, a high-current charged reactor and high-power AC short-circuit generators operated at low power frequency. Except the high-power rectifier test circuit, none of the test circuits can supply the complete stresses to an HVDC CB. However, full-power rectifier test circuits are not available at any test facility yet. In all cases, the rated energy absorption requirement resulting from the required TIV duration, and the lack of DC recovery voltage are the main limitations. Charged capacitor-based test circuits will remain an essential part of research and development. However, a practical test circuit based on a charged capacitor cannot supply rated stresses since the realistic energy that can be stored on a capacitor is limited. Charged reactor-based test circuits can be used to test load current breaking performance of HVDC CBs. It cannot be used for demonstrating short-circuit current interruption performance of several kilo Amperes (kA) since large reactors capable of carrying several kA of current are practically unavailable. Medium sized reactors indeed form an essential part of any test circuits used for testing HVDC CBs.

Finally, the evaluation based on practical aspects singled out the test circuit based on low-frequency AC short-circuit generators, which are available in several laboratories worldwide, as the technically and economically best option to replicate the stresses as in service. The test method exploits the short-circuit making feature at practically any point on the voltage wave to extract a suitable quasi-DC voltage window in a sinusoidally varying AC voltage at low power frequency. Since the power generated by a short-circuit generator is based on mechanical energy stored in its rotating mass, a large amount of electrical energy can be extracted [12], [13]. Nevertheless, testing of HVDC CBs using AC short-circuit generators poses new challenges. For example, large prospective short-circuit current result when the HVDC CB fails to interrupt which could damage not only the device under test but also the test circuit components. The other challenges include the application of a DC recovery voltage after current suppression and transformer saturation due to long duration (DC) TIV during the current breaking process. Pragmatic methods to overcome these challenges are developed and demonstrated in the test laboratory.

A schematic of a complete test circuit based on AC short-circuit generators is shown in Figure 3. The test circuit is composed of four parts: a short-circuit power source (black dashed box), an overcurrent protection circuit (green dashed box), an arcing time prolongation circuit (blue dashed box) and a DC recovery voltage source (red dashed box). The sequence of operation of the switching components in each part is illustrated in [4].

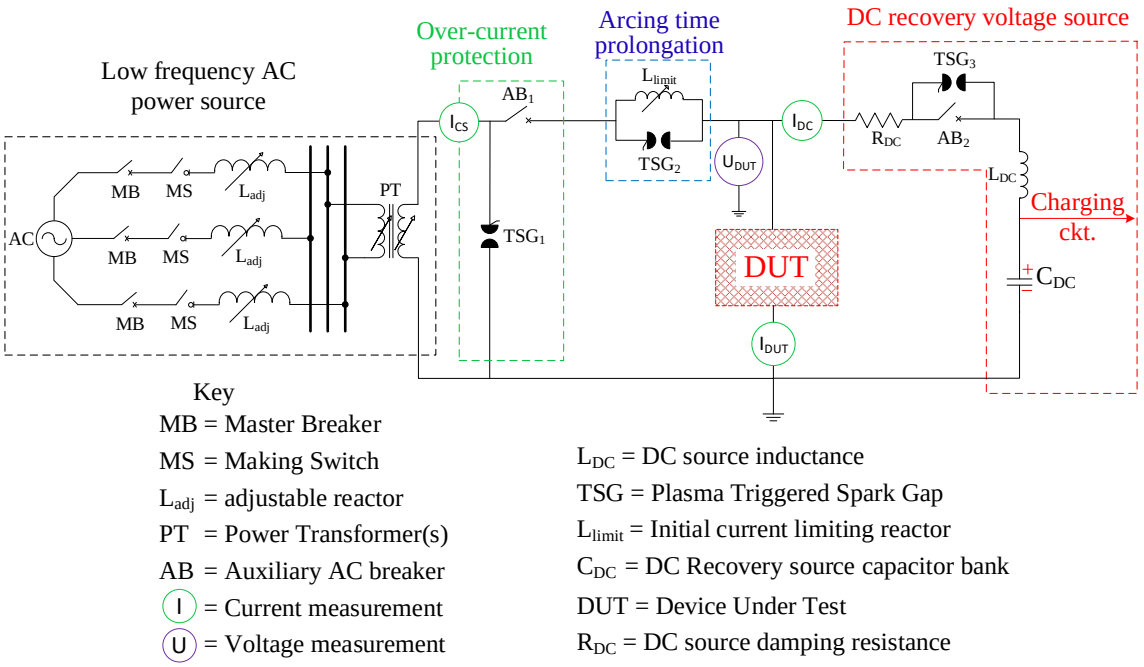

***Figure 3: Schematic of the complete test circuit for testing short-circuit current interruption performance of HVDC CB** [4]*

VI. Performance Demonstrations of HVDC Circuit Breakers

First, the correct functioning of the complete test circuit is verified, and its practical limitations are evaluated. This is carried out by performing tests on prototypes of various technologies of HVDC CBs supplied by OEMs. Then, performance of the HVDC CBs is demonstrated and evaluated from these tests. The test results are discussed below.

a. Test results of active current injection HVDC CB

A prototype of the active current injection HVDC CB rated for 160/200 kV system voltage and 16 kA - TF100 is shown in Figure 4. This breaker consists of two vacuum interrupters in series in the continuous current branch, and pre-charged capacitor bank in series with an inductor and the high-speed making switches (HSMSs, two connected in series) in the current injection branch. The pre-charged capacitor is discharged by closing the HSMSs to inject an (oscillating) counter current which, when superimposed onto the system current, creates local current zeros in the interrupter. A stack of metal oxide surge arrester (MOSA) is placed in parallel to the pre-charged capacitor for energy absorption.

Figure 4: 160/200 kV active current injection HVDC CB prototype

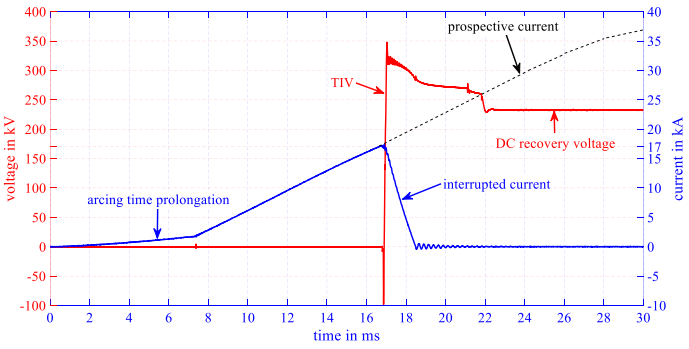

Figure 5: Test Results of active current injection HVDC CB

Figure 5 shows a test result of the active current injection HVDC CB. The same breaker tested for 160 kV system voltage was tested for 200 kV system voltage by modifying the MOSA where the clamping voltage is increased by adding a series MOSA module. To reflect this, the counter current injection capacitor bank is pre-charged to 200 kV, and additional reactors are installed to increase the inductance of the injection circuit in order to maintain the peak value of the injection current as in the 160 kV test case. The breaker interrupts a current of 17.2 kA while producing the TIV with peak value of nearly 350 kV.

It can be seen from the figure that the TIV remains above 300 kV during the entire current suppression period, which lasted for about 1.75 ms. During this period the breaker absorbed nearly 5 MJ energy from the circuit. After the current suppression, the DC recovery voltage of 230 kV (assuming 15% continuous operation overvoltage) is applied (at 22 ms on the graph) for about 1 s. The current suppression is completed around 18.6 ms in the figure. Between 18.6 ms and 22 ms a slightly decaying (due to conduction through the MOSA) self-imposed DC recovery voltage, which is higher than the DC recovery voltage supplied by the test circuit is seen on the graph. This is due to the charge across the capacitor bank of the test breaker that is trapped at the end of the current suppression period. This is because the capacitor remains charged to the same voltage level as the TIV of the breaker during the current suppression period. This breaker has been demonstrated for bidirectional current breaking capability at all defined test duties. The test results of all agreed upon test duties are summarized in Table 2.

Table 2: Summary of tests results of active current injection HVDC CB *[14]*

Test Name	Breaking Current	Δt_{ic} (ms)[4]	Δt_{FS} (ms)[5]	energy (MJ)	DC recovery voltage application	Actual # of tests performed
TC10±[6]	200 A	7	6.5	0.2	180 kV applied	4
TC100±	2,000 A	7	5.5	1.3	180 kV applied	4
TF100±	16 kA	7	1.6	2.6	180 kV applied	4
TDT±	8.5 kA	7	4.3	4.6	180 kV applied	4
TF100[7]	17.2 kA	8	1.6	4	230 kV applied	1

b. Test Results Hybrid HVDC Circuit Breaker

A prototype of a hybrid HVDC CB is also tested using the complete test circuit. The breaker consists of a load commutation switch in series with an ultra-fast disconnector switch in the continuous current branch. In the commutation branch a stack of power electronic switches is used [15]. A photo of the prototype breaker rated at 350 kV system voltage is shown in Figure 6.

Due to the increased rating of the prototype HVDC CB under test, some modifications to the test circuit are needed, for example, in order to take into account the TIV which is in the range of 500 kV. Compared to the test circuit shown in Figure 3, there are three main modifications:

1. Two series connected spark gaps are used for the overcurrent protection instead of one TSG1.
2. AB_1 and AB_2 are, respectively, replaced by double breaking chamber HVAC CBs (rated for 420 kV, 50 kA AC) instead of single breaking chamber HVAC CBs used in other demonstrations.

4 Internal current commutation time [10]
5 Fault current suppression time [10]
6 ± indicates forward and reverse (bidirectional) current interruption
7 This test is performed assuming the system voltage of 200 kV (the system operation voltage in which the breaker can be installed)

The arcing prolongation circuit has been relocated to the grounded side of the DUT in order to avoid excessive terminal-to-ground voltage across this sub-circuit.

Figure 6: 350 kV hybrid HVDC CB prototype

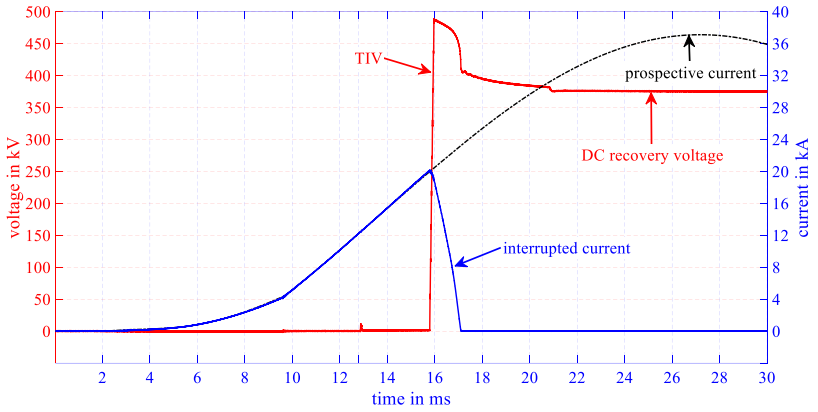

Figure 7: Test result of a 350 kV Hybrid HVDC CB – TF100∗ (20 kA) current interruption test with DC recovery voltage applied

Figure 7 shows a test result of the hybrid HVDC CB prototype, in which the complete test circuit is used. The test result depicts that the prototype breaker suppresses 20 kA current in the test duty TF100∗ while producing a TIV of nearly 490 kV. The prototype breaker produced the TIV after the breaker operation time of 3 ms. It can also be seen that a 380 kV DC recovery voltage (assuming 10% rated continuous overvoltage) is applied after current suppression for about 1 s. The breaker suppresses the fault current from 20 kA to a leakage current level within 1.5 ms.

Table 3 summarizes the test results of all agreed upon test duties. All the test duties have been performed at least twice and in all cases a DC recovery voltage of 380 kV was applied.

Table 3: Summary of test results of 350 kV hybrid HVDC CB prototype *[14]*

Test Name	Breaking Current	Δt_{BO} (ms)	Energy (MJ)	Actual Δt_{FS} (ms)	DC recovery voltage application	# of tests
TC10+[8]	330 A	3	< 1	9.5	380 kV applied	2
TC100+	3,300 A	3	< 7	8.5	380 kV applied	2
TF100+	16 kA	3	10	2.5	380 kV applied	2
TDT+	4.6 kA	3	10.5	9.5	380 kV applied	2
TF100+	20 kA	3	10	1.5	380 kV applied	2

c. Test Results VSC Assisted Resonant Current (VARC) HVDC CB

The VARC HVDC CB consists of an uncharged resonant capacitor similar to the passive oscillation DC transfer switch. However, the main difference is that the L-C resonant circuit in the VARC HVDC CB has a power electronic voltage source in series. Thus, instead of a self-excited oscillation based on the negative dynamic arc resistance of the main interrupter, the excitation of the oscillating current is driven by the voltage source in the commutation branch. Hence, light weight VIs operated by fast actuators can be used as the main interrupter instead of bulky gas CBs. This design uses a full-bridge voltage source converter (VSC) with a low-to-medium voltage (pre-)charged DC link capacitor to excite the oscillating current in the L-C circuit.

[8] + indicates only forward (unidirectional current interruption)

An 80 kV, 12/15 kA VARC HVDC CB consisting of three independent modules connected in series has been tested. The photo of the test setup, including some components of the test circuit, is shown in Figure 8. An important feature in this modular design is that the modules of the CB operate independently from one from another. In this case the breaker operation time of <2 ms and an energy absorption capacity of 3 MJ (1 MJ per module) has been demonstrated [14].

Initially, TF100* of 12 kA was defined and this was successfully achieved within the breaker operation time of 1.5 ms. Later the TF100 is increased to 15 kA which was achieved within the breaker operation time of 2 ms. In both cases the breaker produced a TIV with a peak value of 130 kV while up to 3 MJ energy absorption was demonstrated. The TF100* of 15 kA current interruption was performed for each current direction. Figure 9 shows TF100* forward current interruption in which 15 kA is interrupted within the breaker operation time of 2 ms. The prospective current with a rate-of-rise of nearly 3.5 kA/ms is superimposed for comparison. In this case, the short-circuit current was suppressed within 2.2 ms while absorbing 1.8 MJ of energy. However, DC recovery voltage was not applied from the test circuit during the demonstration of VARC HVDC CB. The decaying DC voltage that is seen after current suppression in the figures is due to the trapped charges across the resonant capacitor which the breaker automatically discharges after current suppression is completed.

Figure 8: 80 kV VARC HVDC CB prototype

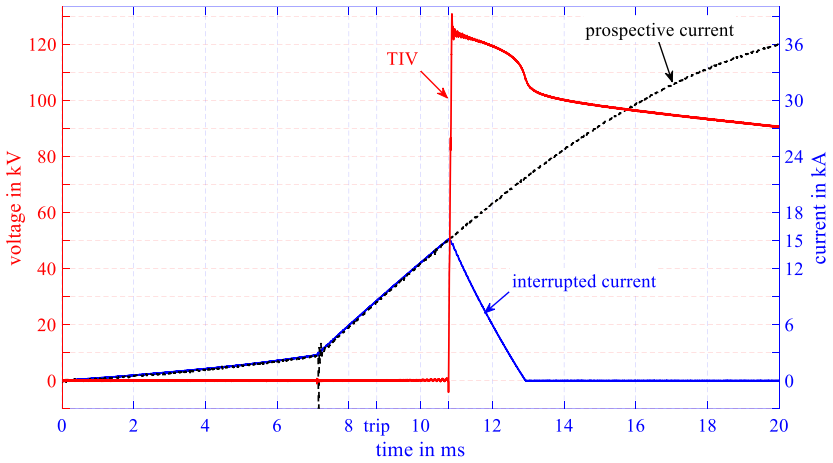

Figure 9: Demonstration of TF100∗ test of an 80 kV VSC assisted resonant current (VARC) HVDC CB

Without increasing energy beyond 3 MJ, sufficient duration TIV is demonstrated by performing test at 8.2 kA current interruption. In this case TIV duration is doubled to 5.3 ms compared 2 ms duration achieved when interrupting 15 kA. In both cases nearly the same amount of energy is absorbed. Table 4 summarizes the list of test duties performed on the 80 kV VARC HVDC CB prototype together with the parameters obtained during test.

Table 4: Summary of test results of 80 kV VARC HVDC CB prototype *[14]*

Test Name	Breaking Current	Δt_{BO} (ms)	Energy (MJ)	Actual Δt_{FS} (ms)	DC recovery voltage application	# of tests
TC10±	200 A	2	0.023	2.6	Not applied	4
TC100±	2,000 A	2	0.16	2.7	Not applied	4

TF100±	12 kA	1.5	1.3	1.9[9]	Not applied	4
TDT±	8 kA	2	2.5	5.3	Not applied	4
TF100±	15 kA	2	1.8	2.2	Not applied	2

VII. Conclusions

Fault situations in a conceptual HVDC grid and the main contributors to the fault current at different stages of the fault current development are investigated via system simulation. Then, the critical stresses on HVDC CBs are identified along with the important stages of the fault current interruption process that need to be reproduced during a short-circuit current interruption test. These stresses are translated into the test requirements and procedures for HVDC CBs. Also, the requirements for a test circuit are specified based on the identified stresses. A test circuit capable of reproducing all the necessary stresses at each stage of the fault current interruption process is proposed and designed, implemented and demonstrated with the testing of the actual industrial prototypes of HVDC CB supplied by three different OEMs. The performance of the following HVDC CBs with voltage and current ratings, and a specified energy absorption and breaker operation time have been demonstrated. These are,

1) Active current injection – parameters 160/200 kV, 16/20 kA, 5 MJ, 7 ms
2) Hybrid – parameters 350 kV, 20 kA, 10 MJ, 3 ms
3) VSC assisted resonant current (VARC) – parameters 80 kV, 12/15 kA, 3 MJ, < 2 ms.

The lessons learned in this project serve as input to the international standardization activities in IEC TC17/WG6 drafting IEC 62271-5 (common specifications for DC switchgear) and IEC TC17A/ WG64 drafting IEC TS 62271-313 (HVDC circuit breakers), Committee Drafts of which are completed. Additional information can be obtained from the work of CIGRE WG A3.40 (on MV DC systems and circuit breakers) and JWG B4A3.80 (on HVDC circuit breakers), both of which will issue Technical Brochures in 2022.

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