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Transient Over Voltage Testing of Cable Systems in MMC-HVDC Links: A Concept Study Including Verification

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SUMMARY

The temporary overvoltages (TOVs) seen by cable system in an HVDC system based on modular multilevel converter (MMC) technology has recently received increasing attention. TOVs in MMC-HVDC systems can occur during transients caused by failures in the system or switching events. The TOVs experienced by the cable system will have different magnitude and wave shape, depending on the location of faults and the converter configurations. The potential impact of the such TOVs on the DC cable system is a major question to both cable manufacturers and transmission system operators. One way, to approach those questions would be experimental investigations. Today, realization of those overvoltages, specifically the long duration overvoltage, using standard high voltage test equipment remains a challenge. Usage of today's impulse generator based test circuits are limited to some tenths of ms decay of the tail voltage.

In this paper, a theoretical study has been conducted to overcome the limitations of today's standard impulse test circuits, and to evaluate possible circuit concepts which potentially could reproduce transient voltages. This has been done for both the long temporary overvoltage (LTOV) as well as the damped oscillatory transient voltage.

Moreover, an experimental set-up on a laboratory scale has been built and evaluated using the presented circuit simulation methods. The presented results show that the physical phenomena of the circuit have been understood. The results have been used to gain knowledge and understanding of the constituting equipment of the proposed circuits, to transfer the test set-up towards higher voltage level application. With this, the paper contributes to the ongoing discussion of testing LTOV and damped oscillatory transient voltages on full scale HVDC cable test circuits.

KEYWORDS

HVDC, XLPE cables, TOVs (temporary over voltages)

1. INTRODUCTION

HVDC extruded cable systems currently experience a tremendous growth in the market of power transmission. Establishing long underground or subsea HVDC links, together with modular multilevel converters (MMC), present a key element in the development of the power grid towards stable and economic integration of renewable energy generation and their distribution over long distances. Given the rapid development of MMC-HVDC converter technology, reinvestigation of occurring temporary overvoltages (TOVs) within MMC-HVDC cables systems has recently gained increasing attention. As an outcome two overvoltage types have been identified within MMC-HVDC point-to-point connections. In case of a DC pole to ground fault, the overvoltage seen by the healthy pole have relatively long duration, from several ms to a few seconds, whereas the faulty pole will see damped zero crossing oscillatory transient voltage. The common test programs according to CIGRE TB 496 and IEC 62895 [1],[2] do not include testing of such TOVs. As a consequence, those overvoltage types found recognition in the new CIGRE Technical Brochures 852 and 853 related to recommendations for respectively extruded and lapped HVDC cable testing [3],[4].

Reproduction of those overvoltages is a desire to develop and understanding of the behavior of the cable system potentially subjected to TOVs. Today's super imposed impulse test circuit typically consists of an impulse generator, an HVDC source, a coupling capacitor or a spark gap, voltage divider as the measurement device, as well as the cable system acting as a capacitive load. Specifically, the impulse generator with its internal front and tail resistors and the impulse capacitor represents key components in extending the impulse shape toward longer wave forms. However, adopting the front and tail resistors has limitations specifically in size and cost. While long impulses with rise / decay times of 7 ms / 25 ms have been achieved earlier, longer tail times of the wave shape are hampered by discharging through the internal resistors of the impulse generator.

This paper deals with the reproduction of those overvoltages using today's standard high voltage laboratory equipment. For this purpose, a theoretical study has been conducted to evaluate possible circuit concepts which potentially could reproduce those transient voltages. The study has been done for both the long transient overvoltage (LTOV) as well as the damped oscillatory transient voltage and is reported in this paper. Moreover, experimental set-ups on laboratory scale have been built and used to evaluate some of the simulated TOV generating circuits.

2. REFERENCE VOLTAGE WAVESHAPE

From the standardization perspective the switching impulse wave shape with rise/decay time of 250/2500 μs has historically been considered sufficient to cover the impact of internal converter faults onto a cable system. Recent studies predict much longer temporary overvoltage (LTOV) types consisting of an initial voltage peak, e.g. 1.8 p.u. with much slower risetime, e.g. up to 10 ms, and a subsequent overvoltage plateau, e.g. 1.6 p.u., which persists up to 100 - 200 ms [5],[6]. The later time is determined by the cable system discharging, either through intrinsic shunt or stray impedances to ground or until auxiliary earthing switches are applied.

A simplified model of the LTOV presented in [7] with peak voltage, U_1 = 2 p.u., with end of peak voltage, U_2 = 1.85 p.u., plateau voltage, U_3 = 1.6 p.u., time to peak, t_1 = 1 ms, time of peak, t_2 = 21 ms, end of plateau, $t_3 \geq$ 150 ms, time of decay after the plateau to U_0 = 1 p.u. or ground $t_4 \geq$ 300 ms. A typical peak level of U_1 = 2 p.u. has been selected as a targeted value to account for a 15% margin in testing schemes compared to predicted occurring overvoltage's as specified in the standard [1]. The described wave shape of LTOV is depicted in Figure 1.

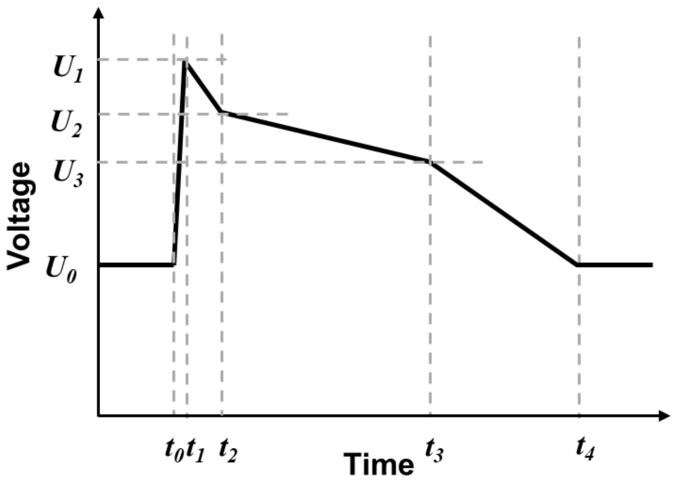


Figure 1 : Target LTOV extracted from [7].

The main challenge here is how to generate such a wave shape in the laboratory conditions to test a cable system. The other challenge lies in the availability of test equipment itself and on the measurement of such impulse waveshape with current measurement techniques or instrument. Feasibility study has been performed to generate the switching impulse of long front and tail times of few ms with the existing test equipment [8]. The study has given some insight to understand the challenges or limitations with respect to generate and to test the LTOV in the laboratory. In the following sections of this paper these challenges and limitations are addressed.

3. SIMULATION RESULTS

In this section several circuit concepts have been simulated with the target of generating a long temporary over voltage (LTOV) depicted in Figure 1 as well as a damped oscillatory transient voltage. For the simulations Spice circuit simulation software has been used. The different circuit concepts of LTOV are separated in concepts including the usage of an impulse generator and in concepts not relying on an impulse generator, instead utilizing two DC sources.

3.1 Impulse Generator Based Circuit Concepts

The common test concept or circuit to generate transient of impulse nature is using the impulse generator. Simulation studies were performed to understand the limits with the standard test equipment and to check the possibilities to generate the LTOV with the impulse generator based test circuit. Figure 2 shows the schematic of the test setup for generating the superimposed standard switching impulse or lightning impulse. The test circuit typically consists of an impulse generator, an HVDC source, a coupling capacitor or a spark gap to protect the impulse generator from high voltage DC, a voltage divider as the measurement device, a test object, typically represented through its capacitance, and a protection resistor to protect the DC source from cable discharge. Specifically, the impulse generator with its internal front and tail resistors and the impulse capacitor represents key components in generating the required impulse shape. The desired time to peak and the half time of the double exponential impulse waveform can be achieved by adjusting the front or damping resistance and tail or discharge resistance and the per stage capacitance. The time to peak of the impulse can be increased by adding an external damping resistor in series with the impulse generator and the time to half can be increased by increasing the per stage capacitance and discharge resistance. Both methods have limitations with respect to the maximum values and has significant effect on the overall performance of the impulse generator. The addition of an external damping resistor results in a decrease of the overall efficiency of the impulse generator, whereas increase in per stage capacitance and discharge resistance have limitations with respect to availability of (few kΩ) resistors, mechanical connections and space within standard impulse generators.

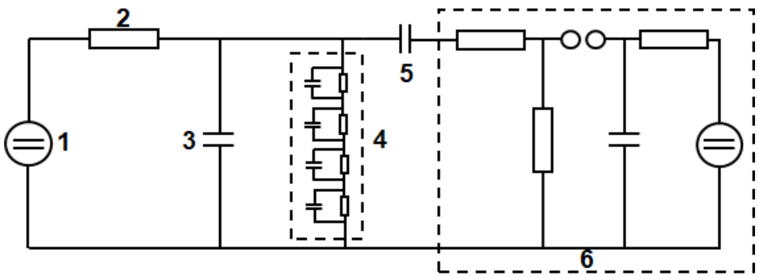


Figure 2. Schematic of the test setup for generating the standard switching impulse. 1. HVDC source, 2. Protection resistor, 3. Cable, 4. Voltage divider, 5. Coupling capacitor, 6. Impulse generator

Investigation has been performed in earlier publication [8] with the dimensioning of the impulse generator i.e., by adapting the front and tail resistors and per-stage capacitance of the impulse generator. The experimental setup and the test concept were successfully verified including a successful full-scale test performed on a 320 kV and 525 kV cable system [8],[9]. The double exponential impulse wave with a time to peak of up to 8 ms and a time to half of up to 25 ms was achieved.

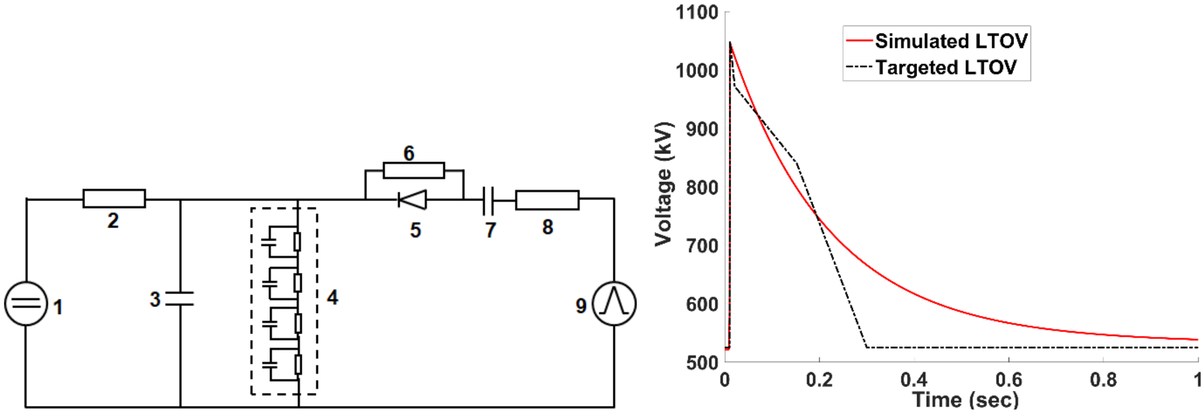
Additional prototype tests have been performed to check the limits with this test concept. A test was performed with the available state-of the-art components and configuration of the impulse generator at hand. A maximum time to half of up to 60 ms was achieved by appropriately adapting the front and tail resistors and per-stage capacitance of the impulse generator. Though with this test concept significantly long tail times was achieved, the maximum value is far from the targeted decay times of 100 to 200 ms.

With a standard test circuit with impulse generator it will not be possible to generate a desired LTOV. The main challenge comes from the discharge of the load through the impulse generator and that limits the maximum tail or decay time of the impulse. To avoid discharging of the load through the impulse generator, a set of high value resistors to be used, which is not practically possible with the existing impulse generator configurations.

An alternative solution would be needed to prevent the discharging of the load through the impulse generator to extend the decay time. One of the solutions is adding a diode in series with the impulse generator. The use of diode takes away the limitations of internal charging resistors, that also discharge the impulse, as diode prevent the flow of charge from the load to the impulse generator and hence gives a fixed limit to the longest possible tail time. The similar test concept was successfully tested in lab scale and the results were published [10].

Figure 3.a shows the schematic of the test setup for generating the LTOV with the test concept of impulse generator in series with the diode. The cable is pre charged to the desired DC voltage level by the DC generator. The impulse from the impulse generator is applied to the cable through the coupling capacitor. As the diode is in series with the impulse generator, the charging and discharging of the cable through the impulse generator is possible only as long as the current flows in one direction from impulse generator to cable through the diode. As soon as the charging voltage of the cable is more than the output voltage of the impulse generator, the direction of the current changes and the diode stops conducting. The cable start discharging through the voltage divider and the external discharge resistor. In that way, the long tail time of the impulse is achieved. The magnitude of tail time is mainly determined by the branch resistors of the voltage divider and the external discharge resister. The time to peak of the impulse is mainly determined by the cable capacitance, coupling capacitance, internal and external damping resistor and can be therefore easily adjusted.

Figure 3.b shows the simulation results of the impulse curve with test concept of impulse generator in series with diode for a level of U_0 of 525 kV in comparison with the targeted LTOV as depicted in Figure 1. For the simulated test circuit parameters, the simulated curve showed longer tail times, i.e. targeted plateau or tail time of $t3 \geq 150$ ms. The peak and the rise of the pulse has been selected to comply with the peak U_1, t_1 of the reference curve. However, the overshoot of the reference model curve cannot be resolved by this circuit. Additionally, one of the challenges with this test concept is the availability of the high voltage diode with specific requirements such as maximum reverse voltage, maximum forward peak current, and short reverse recovery time.

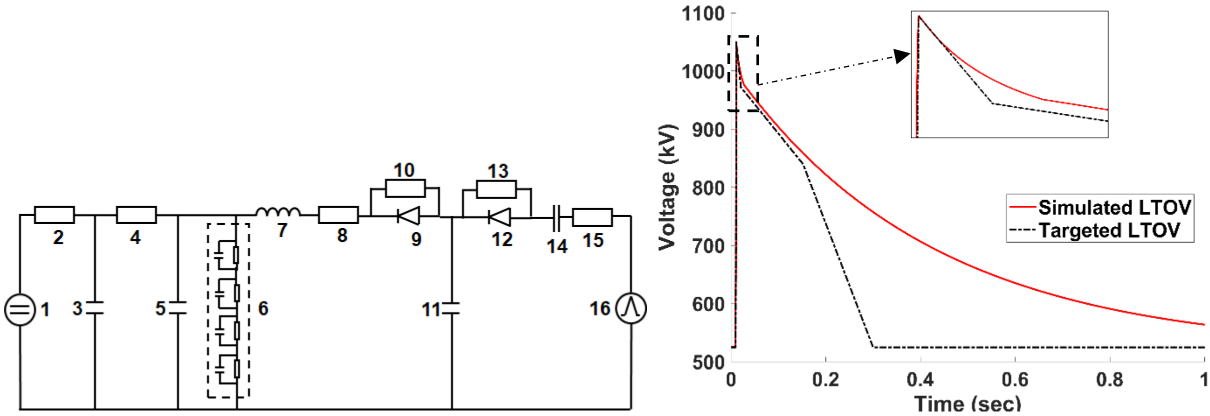


(a) *(b)*

Figure 3. (a) Schematic of the test setup for generating the LTOV with impulse generator and diode. 1. HVDC source, 2. Protection resistor, 3. Cable, 4. Voltage divider, 5. High voltage diode, 6. Discharge resistor, 7. Coupling capacitor, 8. External Front resistor, 9. Impulse generator. (b) Simulated LTOV in comparison with targeted impulse.

Though the test concept of impulse generator in series with diode could produce double exponential impulse with longer tail times, generating the initial peak overshoot with peak time of t_2 and maintaining the controlled plateau from t_2 to t_3 is not possible. In general this is a difficulty with the double exponential type impulse curve, where the time to half or plateau time is determined by the time to peak, i.e. a small change in the time to peak could affect the desired tail time. This challenge could be overcome by an impulse with peak overshoot with two different decay times. Where the time to peak, peak time and plateau times are independent of each other and would be controlled by the different circuit parameters.

Further studies have been performed to achieve an LTOV including an initial overshoot with a certain peak voltage. Figure 4.a shows the schematic of a test setup for an LTOV with peak overshoot utilizing an impulse generator. For this, an additional reactor is connected in series with the impulse generator and diode circuit along with the additional discharge resistor and capacitors. The series reactor, the peak overshoot capacitor and the discharge resistors controls the initial peak decay to generate defined peak time t_2. The plateau time is controlled by the cable discharge through the tail resistor and branch resistance of the voltage divider.



(a) *(b)*

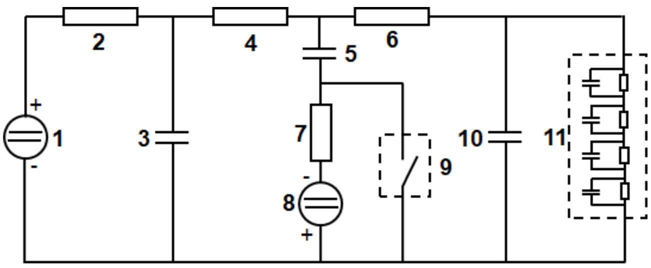
Figure 4. (a) Schematic of the test setup for generating the LTOV with impulse generator, diode and reactor. 1. HVDC source, 2. Protection resistor, 3. Filter capacitor, 4. Tail resistor, 5. Cable, 6. Voltage divider, 7. Reactor for peak overshoot, 8, 10 & 13. Discharge resistors, 9 & 12. Low voltage diodes, 11. Capacitor for peak overshoot, 14. Coupling capacitor, 15. External front resistor, 16. Impulse generator. (b) Simulated LTOV in comparison with targeted impulse.

Figure 4.b shows the simulation results of the impulse curve with test concept of impulse generator in series with diode and reactor for 525 kV nominal voltage in comparison with the targeted LTOV. For the simulated test circuit parameters, the simulated curve showed the peak overshoot with peak time of $t_2 > 21$ ms and targeted plateau or tail time of $t_3 \geq 150$ ms. After the plateau, the voltage discharges back to 1 p.u. (pre-DC voltage level) either by following the plateau decay or by forcing down the faster decay with an external discharge circuit (not shown in this circuit).

3.2 DC Source Based Circuit Concepts

Instead of utilizing an impulse generator for generation of the LTOV two DC sources can be used, where one source is coupled to the test object by a capacitance. The long overvoltage is generated by grounding one DC source, after the coupling capacitor has been charged to the nominal voltage of opposite polarity. The advantage of this circuit is the slower discharging of the test object compared to a circuit with impulse generator, which has inherently a resistive grounding path. The logic of this circuit may be compared to a real HVDC point-to-point link, e.g. in a symmetric monopolar configuration. Here the converter may act towards the cable poles as DC sources and the poles are coupled through the inherent capacitance of the, e.g. half-bridge, converter cells. In case of a pole-to-ground fault the capacitance of the converter cells leads to an increase in voltage of the other healthy pole towards almost the double voltage, respectively a level determined by the arrester protection of the system. A plateau will build up until both AC breakers of the link are opened and interrupt any energy infeed. Discharging of the pole can only occur through the generally low converter resistance, until further protection equipment will allow for faster discharge.

A schematic diagram of a circuit concept is shown in Figure 5.a, where the focus is on reproducing a plateau as in the reference pulse of Figure 1, respectively long tail times. For this, the two DC sources of different polarity are coupled via a coupling capacitor to the test object. Each DC source again is protected by a resistor from cable discharge, and a grounding switch is added in parallel to one of the DC sources. Under charging of the coupling capacitor, the switch is open. The circuit parameters to be chosen such that the nominal voltage, which is essentially supplied through the first DC source, applies to the test object. At the same time the voltage drops over the coupling capacitance, which is supported from the second DC source, needs to resemble the desired TOV peak. For generation of the TOV the grounding switch will be closed, which automatically lift the voltage of the other side of the coupling capacitor towards the desired TOV level. The grounding switch can be a sphere gap or a breaker. Due to better controllability a breaker would be preferred. Additional resistors in the main current path allow for tuning the tail and the front time.



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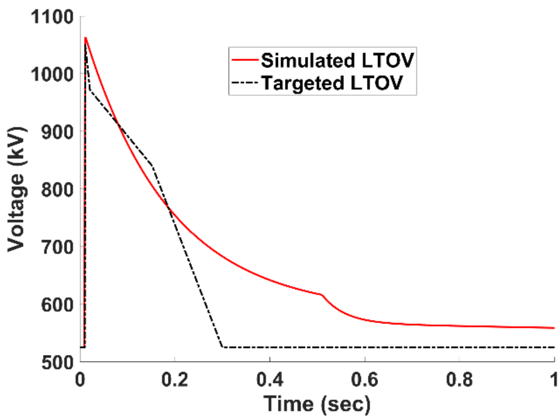
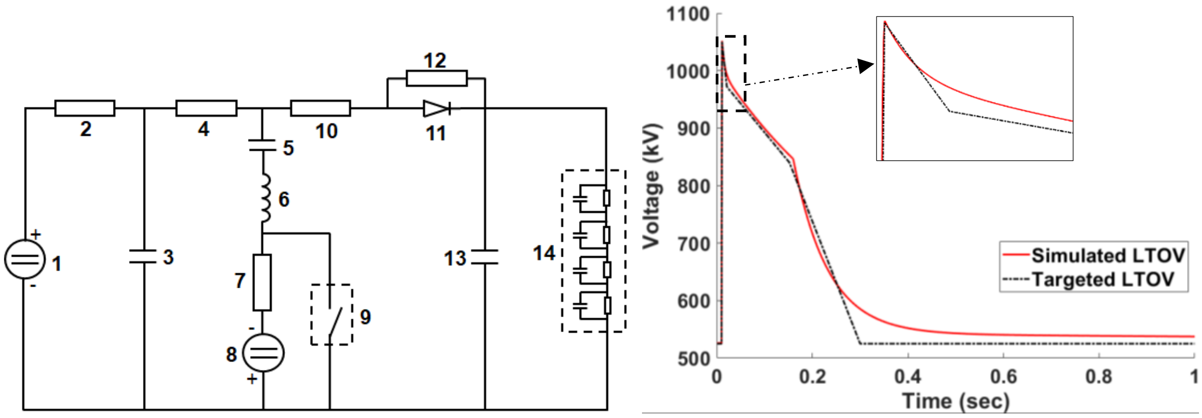


(b)

Figure 5: (a) Schematic of the test setup for generating the LTOV with two DC sources. 1. HVDC source, 2. Protection resistor, 3. Filter capacitor, 4. Tail resistor, 5. Coupling capacitor, 6. Front resistor, 7. Protection resistor, 8. HV DC Source, 9. Switch (sphere gap/breaker), 10. Cable, 11. Voltage divider. (b) Simulated LTOV in comparison with targeted impulse.

The simulation results for the 525 kV test circuit is shown also in Figure 5.b and compared to the reference model curve of the LTOV from Figure 1. While the overshoot of the reference model curve cannot be resolved by this circuit, the peak and the rise time of the pulse has been selected to comply with the peak U_1, t_1 of the reference curve. The tail resistance has been chosen to avoid an overstress compared to the reference curve leading to a value of U_3 being approximately 1.5 p.u. at the end of the plateau t_3 of the reference curve.

Similar to the concept including an impulse generator the reproduction of the initial overshoot can be achieved. One way of doing it is by adding a low voltage diode with discharge resistor and a reactor. Such a circuit is depicted in Figure 6.a. With this an additional decay time scale is introduced, which can be controlled through the discharging resistor over the diode. The circuit parameter setting in the simulation of Figure 6.b is such that the peak voltage coincides with the reference LTOV curve, the simulated peak overshoot has a peak time of $t_2 > 21$ ms and targeted plateau or tail time of $t_3 \geq 150$ ms. After the plateau, at the time of approximately $t_3 = 200$ ms, the grounding switch is closed again, causing a potential change of one side of the coupling capacitor. In the consequence the potential over the test object will be pulled again towards the initial level and the test object will discharge into the coupling capacitor back to 1 p.u. (pre-DC voltage level).



(a) (b)

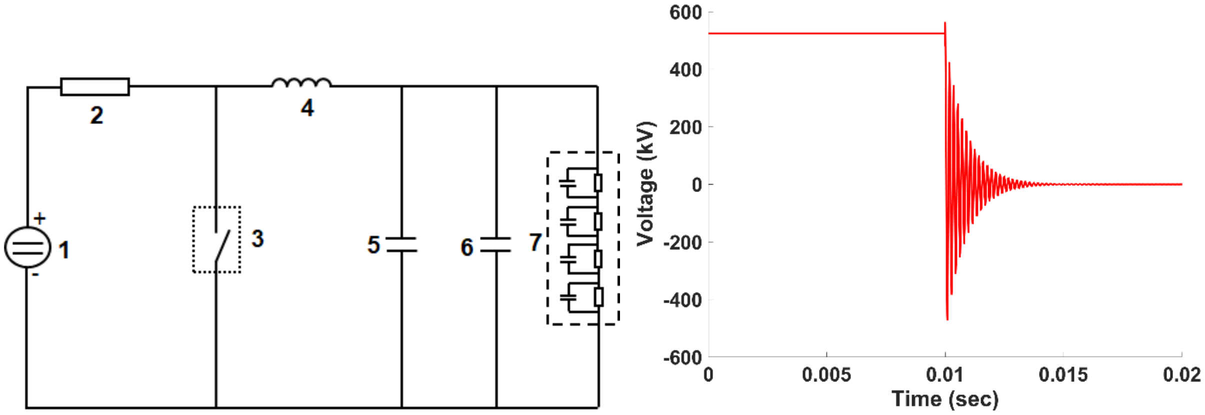
Figure 6: Schematic of the test setup for generating the LTOV with two DC sources, diode and reactor. 1. HVDC source, 2. Protection resistor, 3. Filter capacitor, 4. Tail resistor, 5. Coupling capacitor, 6. Reactor for peak overshoot, 7. Protection resistor, 8. HVDC Source, 9. Switch (sphere gap/breaker), 10. Front resistor, 11. Low voltage diode, 12. Peak decay resistor, 13. Cable, 14. Voltage divider. (b) Simulated LTOV in comparison with targeted impulse.

Overall, this circuit concept leads to an excellent agreement with desired target curve from Figure 1, which eventually is seen as representing real system signals in a good way. Ultimately, the authors believe, there are even more ways of realizing related LTOV shapes.

3.3 Damped Zero Crossing Oscillations

Damped zero crossing oscillations type transient voltage of different frequency can be generated in the high voltage laboratory with a series R-L-C damped circuit in series with a fixed DC source and a grounding switch. There are some different circuit approaches to generate the test curve based on the connection of the circuit components. Figure 7.a shows the schematic of one of the test concepts for generating the damped zero crossing oscillations with different frequency. To generate a test curve, the cable must be pre-charged by a DC source and then discharged. The cable will be discharged through a reactor by triggering the grounding switch. For the grounding switch, either a sphere gap or a breaker can be used. The simulations were performed with a breaker as grounding switch. The damping of the oscillations is determined by the series resistance of the reactor. As an option an additional resistor can be connected in series with the reactor to adjust the damping of the oscillations. The protection resistor is used to avoid an over current trip of the DC generator during the discharge of the cable. The frequency of the oscillations can be adjusted by choosing the right value of the reactor. An additional capacitor in parallel to the cable would be needed to generate the low frequency oscillations. Adding an additional capacitor has the advantage that cable length or losses does not affect the frequency or the attenuation of the oscillation. For higher frequencies one may not require having an additional capacitor, instead a reactor with higher inductance can be used. One important observation from the simulations is that there may be a fast transient of high voltage over the reactor in the oscillation tests, so the reactor needs to be dimensioned to withstand the high voltage transients. This is due to external connection inductances and stray capacitances over the reactor (not shown in the figure).

Figure 7.b shows the simulation results of the damped zero crossing oscillation with frequency of 5.7 kHz. For the simulated test circuit parameters, the first opposite peak has an amplitude of >90% of U0 (pre-DC stress) and >14 oscillations to reach the amplitude below 5% of U0.



(a) *(b)*

Figure 7. (a) Schematic of the test setup for generating the damped zero crossing oscillations. 1. HVDC source, 2. Protection resistor, 3. Switch (sphere gap/breaker), 4. Reactor for oscillations, 5. Capacitor for oscillations, 6. Cable, 7. Voltage divider. (b) Damped zero crossing oscillation with frequency of 5.7 kHz.

4. EXPERIMENTAL SETUP AND RESULTS

Laboratory scale tests have been performed to verify the simulated test concept presented, both on the generation of a LTOV as well as on the generation of the damped zero crossing oscillation type of TOV. The test results are presented in the following section.

4.1 LTOV

A laboratory scale test was performed utilizing the simulated test concept presented in Figure 6. Based on the available voltage level of the lab scale test components, the DC prestress voltage was chosen to 52.5 kV, i.e. 1/10 of the planed 525 kV DC level, with targeted peak impulse of 2 p.u., i.e. 105 kV. Figure 8 shows the schematic of the test circuit to generate LTOV in the laboratory. The test was performed on a capacitive load with capacitance equivalent to the targeted cable capacitance. A sphere gap of diameter 250 mm was used as the grounding switch for the lab scale test. The gap between the spheres was adjusted by the motor-controlled mechanism to be able to easily trigger the gap. However, a sphere gap may have limitations compared to a breaker, specifically during long switching times. The main challenge is to maintain the arc for the specified time as the arc may extinguish for low discharge currents. During the test, it was seen that the sphere gap turned off the current too early. In order to provide enough current to keep the arc conducting during the whole impulse, RC elements were connected in parallel over the sphere gap as shown in Figure 8.

To generate a targeted front time of 1 ms with peak overshoot, a peak overshoot reactor of 6.5 H and front resistor of 26 kΩ were needed to be connected in the circuit. Instead, based on availability of test components in the laboratory, a peak overshoot reactor of 1.17 H and front resistor of 11 kΩ was used for the lab scale tests. Simulations were performed with this low value of reactor and front resistor, and a front time of 0.4 ms was shown by the simulation results. For the RC circuit supporting the sphere gap a 0.25 µF impulse capacitor and a 287 kΩ high voltage resistor was used. Figure 9.a shows the image of test setup build to generate a LTOV in the laboratory.

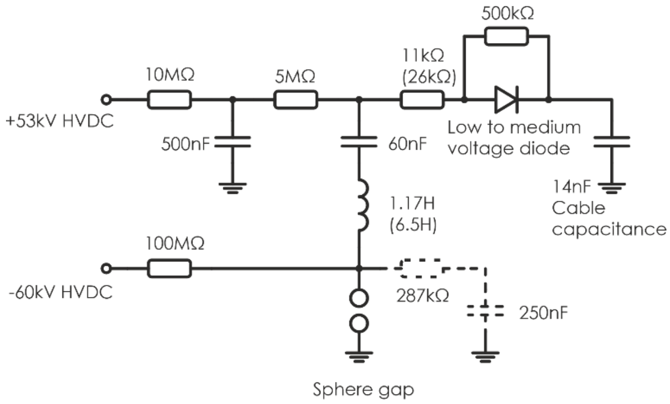
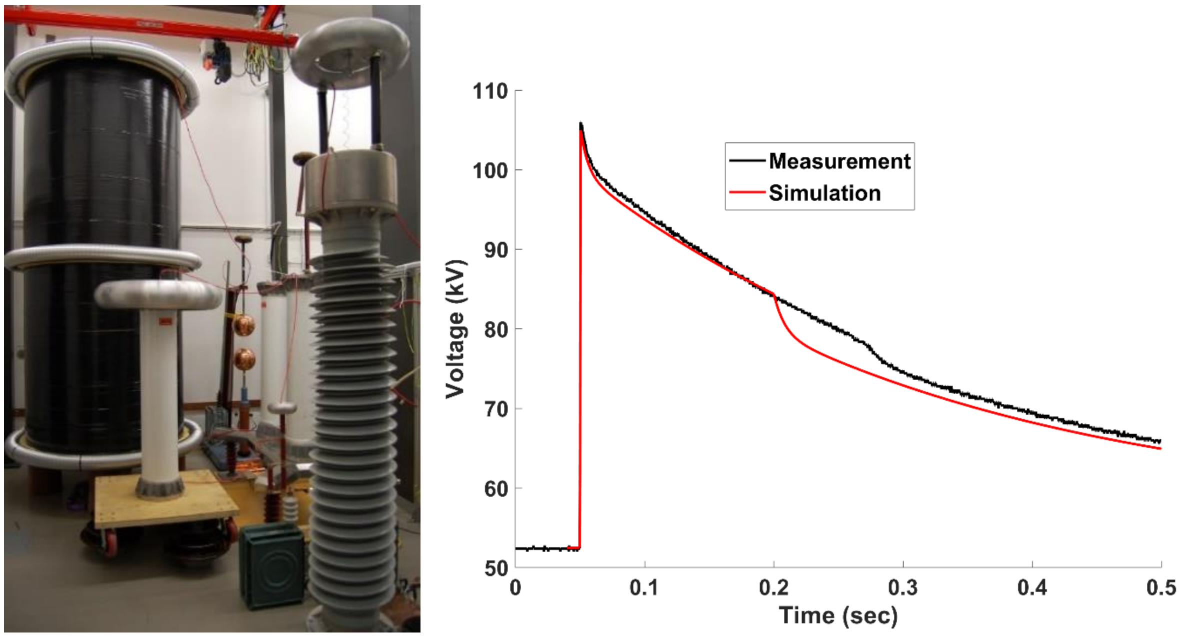


Figure 8. Test circuit to generate LTOV in the laboratory.

Figure 9.b shows the measured and simulated curve of the LTOV. A good match between them was observed. The targeted LTOV with end of plateau of $t_3 \geq 150$ ms was achieved. In Figure 9.b the measured impulse curve shows longer decay time than the simulated curve. This observed longer decay time originated from the RC circuit maintaining the conduction of the sphere gap for the longer time. However, a better control on decay time of the impulse can be achieved by replacing the sphere gap with an appropriate breaker. A faster decay after switch opening is achieved without RC circuit in parallel to the sphere gap.



(a) (b)

Figure 9. (a) Test setup to generate LTOV in the laboratory. (b) Measured and simulated results over a dummy capacitor with typical load parameters of a cable for LTOV.

4.2 Damped Zero Crossing Oscillations

Figure 10 shows the test circuit for the generating damped zero crossing oscillation type TOV with frequency of 5.7 kHz. The circuit consists of 10 MΩ protection resistor along with the reactor of 1.6 mH with an AC series resistance of 0.23Ω and the load capacitance of 500 nF. A sphere gap of diameter 250 mm was used as the grounding switch. Several lab scale tests were performed to understand the conduction of the sphere gap and minimum discharge current to maintain the arc for zero crossing oscillations. No issues with the conduction of sphere gap was observed with the tested frequency ranges from 200 Hz to 5.7 kHz. The test was performed at DC prestress of 40 kV. The voltage was chosen to avoid any damage to the measuring device, such as current sensor due to high current from the high frequency oscillations. The load capacitor was charged to a voltage of 40 kV and discharged through the reactor and grounded sphere gap. Figure 11.a shows the image of test setup built to generate a damped zero crossing oscillations with frequency of 5.7 kHz in the laboratory.

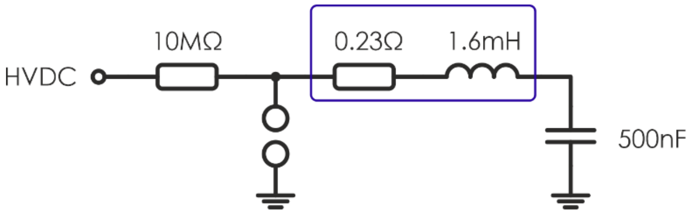
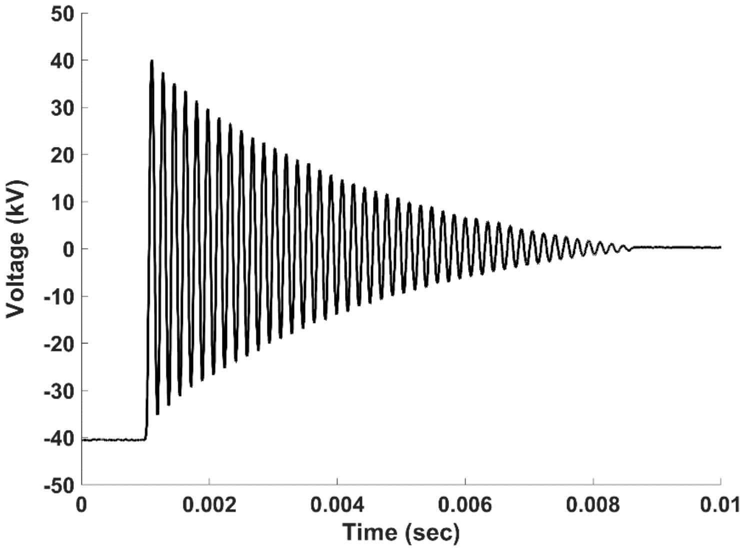


Figure 10. Test circuit to generate damped zero crossing oscillations in the laboratory

Figure 11.b shows measured curve of the damped zero crossing oscillation type TOV with frequency of 5.7 kHz. For the chosen test circuit parameters, the TOV with the first opposite peak of an amplitude close to 1 p.u. i.e. > 90% of U_0 and 36 oscillations to reach the amplitude below 5% of U_0 was achieved.



(a) *(b)*

Figure 11. (a) Test setup to generate damped zero crossing oscillations of frequency 5.7 kHz with circuit concept presented in Figure 7. (b) Measured results over a dummy capacitor for damped zero crossing oscillations of frequency 5.7 kHz.

5. CONCLUSION AND OUTLOOK

Recently a new type of temporary overvoltage has been introduced into the discussion concerning stresses experienced by HVDC cable systems; namely the long temporary overvoltage and the damped oscillating transient overvoltage, which were described in more details in this paper. They have also been mentioned in the latest release on recommendations for testing DC extruded/lapped cable systems for power transmission, namely CIGRE Technical Brochure 852/853. Still, there are technical hurdles and suspicion on how to generate, specifically the LTOV type of voltage stress for testing purposes utilizing HV laboratory test equipment. In this paper at least four concepts have been disclosed to overcome those obstacles. Two of them based on utilization of today's stat-of-the-art impulse generator, and two concepts utilizing two DC sources for LTOV generation. With at least two of the concepts, even different time scales can be introduced into the same pulse shape to account for e.g. peaks or overshoots. Simulations have been performed with the different circuit concepts and compared to a reference LTOV curve, where the latter has been deduced from literature. Overall, the simulation and the targeted TOV curves are shown to be in good agreement, indicating that generation of the investigated overvoltage types, namely the LTOV and the damped zero crossing oscillatory transient voltage will be possible at commercially relevant voltage levels. Moreover, excellent agreement has been found, e.g. for the concept utilizing two DC sources including a reactor, diode, discharge resistor combination to capture overshoots. For this concept also the practical feasibility has been demonstrated in an HV experiment with 52.5 kV nominal and 105 kV peak voltage. The simulation for this experiment has been found to be in good agreement with the measured curve, demonstrating also that the effects and couplings in the circuit. This is especially important for the last step in upscaling to, e.g. 525 kV voltage level. Besides the LTOV, a simulated concept has been also proposed for the damped oscillation transient overvoltage, including its experimental verification. The experimental demonstration was done on a nominal voltage level of 40 kV.

As an outlook it shall be mentioned, that providing actual test circuits for the generation of, e.g. an LTOV curve, is not enough. Additionally, control of the pulse shapes by the parameter settings, variation of pulse shapes, and respective measurement and analysis of it remains to be addressed. This is important to guarantee reproducibility of the test wave shape. A first introduction to the problem is presented in [11]. There, the importance of the voltage measurement and related analysis of the measured data is emphasized, utilizing the example of an impulse generator based test circuit with double exponential wave form. Due to a strong interrelation of front and decay times in such a circuit concept, variations within the allowed tolerances for measuring the peak voltage might lead to widely varying decay times. As a consequence, reproducibility is difficult to achieve. Such phenomena are expected to be much less pronounced in circuit concepts with two DC sources. The absences of such strong interrelations between different sections within the LTOV profile, fluctuations in the pulse shape measurements have only little impact on the final pulse shape. Instead different time scales of the stress curve can be controlled rather independently by the different sections in the circuit, which potentially might simplify reproducibility and minimize variations.

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